CLAIMS

1. A method for communicating between a controller and a device with double-buffered inputs, the method comprising the steps of:

(a) providing one or more communication paths for exchanging data between the controller and the device;

(b) providing a data transfer control signal from the controller to the device for transferring input data from one or more input registers into one or more latchable data registers; and

(c) providing a data transfer delay signal from the device to the controller, wherein, in a first logic state, the data transfer delay signal prevents transfer of input data from said one or more input registers into said one or more latchable data registers until after a transition to a second logic state occurs on the data transfer delay signal.

2. The method in accordance with claim 1, wherein the step (a) of providing one or more communication paths further comprises providing a serial data communication line and a serial clock signal communication line.

3. The method in accordance with claim 2, wherein the serial data communication line is a bi-directional data communication line.

4. The method in accordance with claim 1, wherein the step (a) of providing one or more communication paths further comprises providing a parallel data bus and parallel data transfer control signals.

5. The method in accordance with claim 4, wherein the parallel data bus is a bi-directional parallel data bus.

6. The method in accordance with claim 1, wherein the step (b) of providing a data transfer control signal further comprises providing a data transfer control signal that latches input data from the input registers into the latchable data registers on a high-to-low logic level transition.

7. The method in accordance with claim 1, wherein the step (b) of providing a data transfer control signal further comprises providing a data transfer control signal that is held at a first logic level such that completion of a write operation to an input register controls latching of input data into the latchable data registers, subject to delay introduced by the data transfer delay signal.

8. The method in accordance with claim 1, wherein the step (c) of providing a data transfer delay signal from the device to the controller further comprises the step of providing an open-drain data transfer delay signal between the device and the controller.

9. The method in accordance with claim 8, wherein the open-drain data transfer delay signal is coupled to an internal buffer that generates a BUSY input signal on the device that prevents transfer of input data from said one or more input registers.

10. The method in accordance with claim 9, wherein the device comprises multiple devices and the open-drain data transfer delay signal is coupled to other data transfer delay signals from other similar devices to realize a system-wide data transfer delay signal.

11. Apparatus for communicating between a controller and a device with double-buffered inputs comprising:

means for providing one or more communication paths for exchanging data between the controller and the device;

means for providing a data transfer control signal from the controller to the device for transferring input data from one or more input registers into one or more latchable data registers; and

means for providing a data transfer delay signal from the device to the controller, wherein, in a first logic state, the data transfer delay signal prevents transfer of input data from

said one or more input registers into said one or more latchable data registers until after a transition to a second logic state occurs on the data transfer delay signal.

12. The apparatus of claim 11, wherein the means for providing one or more communication paths further comprises a serial data communication line and a serial clock signal communication line.

13. The apparatus of claim 12, wherein the serial data communication line is a bi-directional data communication line.

14. The apparatus of claim 11, wherein the means for providing one or more communication paths further comprises a parallel data bus and parallel data transfer control signals.

15. The apparatus of claim 14, wherein the parallel data bus is a bi-directional parallel data bus.

16. The apparatus of claim 11, wherein the means for providing a data transfer control signal further comprises means for providing a data transfer control signal that latches input data from the input registers into the latchable data registers on a high-to-low logic level transition.

17. The apparatus of claim 11, wherein the means for providing a data transfer control signal further comprises means for providing a data transfer control signal that is held at a first logic level such that completion of a write operation to an input register controls latching of input data into the latchable data registers, subject to delay introduced by the data transfer delay signal.

18. The apparatus of claim 11, wherein the means for providing a data transfer delay signal from the device to the controller further comprises means for providing an open-drain data transfer delay signal between the device and the controller.

19. The apparatus of claim 18, wherein the open-drain data transfer delay signal is coupled to an internal buffer that generates a BUSY input signal on the device that prevents transfer of input data from said one or more input registers.

20. The apparatus of claim 19, wherein the device comprises multiple devices and the open-drain data transfer delay signal is coupled to other data transfer delay signals from other similar devices to realize a system-wide data transfer delay signal.

21. A communications interface for enabling communication between a controller and a device with double-buffered inputs, the communications interface comprising:

one or more communication paths for exchanging data between the controller and the device;

a data transfer control signal from the controller to the device for transferring input data from one or more input registers into one or more latchable data registers; and

a data transfer delay signal from the device to the controller, wherein, in a first logic state, the data transfer delay signal prevents transfer of input data from said one or more input registers into said one or more latchable data registers until after a transition to a second logic state occurs on the data transfer delay signal.

22. The communications interface of claim 21, wherein said one or more communication paths comprise a serial data communication line and a serial clock signal communication line.

23. The communications interface of claim 22, wherein the serial data communication line is a bi-directional data communication line.

24. The communications interface of claim 21, wherein the data transfer delay signal from the device to the controller comprises an open-drain data transfer delay signal coupled to an internal buffer that generates a BUSY input signal on the device that prevents transfer of input data from said one or more input registers.

25. The communications interface of claim 24, wherein the device comprises multiple devices and the open-drain data transfer delay signal is coupled to other data transfer delay signals from other similar devices to realize a system-wide data transfer delay signal.

26. A method for communicating between a controller and multiple data conversion devices, each of said data conversion devices including multiple DACs with double-buffered inputs, the method comprising the steps of:

(a) providing a bi-directional serial data communication line and a serial clock signal communication line for exchanging data between the controller and the data conversion devices;

(b) providing a data transfer control signal from the controller to the data conversion devices that latches input data from input registers into interconnected latchable data registers of associated DACs on an active transition;

(c) providing open-drain, bi-directional data transfer delay signals in a wired-OR configuration from the data conversion devices to the controller, wherein, in a first logic state, the data transfer delay signal prevents transfer of input data from said input registers into said latchable data registers until after a transition to a second logic state occurs on the data transfer delay signal;

such that, when any of the data conversion devices drives the data transfer delay signal to said first logic state, transfer of input data from said input registers into said latchable data registers is inhibited in every DAC in every data conversion device that is part of the wired-OR configuration.